

WHAT IS CLAIMED IS:

- 1 1. A composite spacer for use with a split gate flash memory cell on a substrate, comprising:
 - 2 a first spacer insulating layer having a first deposition distribution that varies as a
 - 3 function of a location of said split gate flash memory cell on said substrate; and
 - 4 a second spacer insulating layer overlying said first spacer insulating layer and having a
 - 5 second deposition distribution that varies in substantial opposition to said first deposition
 - 6 distribution of said first spacer insulating layer as a function of said location of said split gate
 - 7 flash memory cell on said substrate.
- 1 2. The composite spacer as recited in Claim 1 wherein said composite spacer forms a
- 2 composite floating gate spacer proximate a floating gate of said split gate flash memory cell.
- 1 3. The composite spacer as recited in Claim 1 wherein said first spacer insulating layer
- 2 forms a thicker composition proximate a center of said substrate and a thinner composition
- 3 toward an edge of said substrate and said second spacer insulating layer forms a thinner
- 4 composition proximate said center of said substrate and a thicker composition toward said edge
- 5 of said substrate.
- 1 4. The composite spacer as recited in Claim 1 wherein said split gate flash memory cell is
- 2 located proximate a center of said substrate, said first spacer insulating layer having a thicker
- 3 composition and said second spacer insulating layer having a thinner composition.
- 1 5. The composite spacer as recited in Claim 1 wherein said first spacer insulating layer is
- 2 formed by a low pressure tetraethyl orthosilicate layer and said second spacer insulating layer is
- 3 formed by a plasma enhanced tetraethyl orthosilicate layer.

1 6. A method of forming a composite spacer for use with a split gate flash memory cell on a
2 substrate, comprising:

3 providing a first spacer insulating layer having a first deposition distribution that varies as
4 a function of a location of said split gate flash memory cell on said substrate; and
5 depositing a second spacer insulating layer over said first spacer insulating layer, said
6 second spacer insulating layer having a second deposition distribution that varies in substantial
7 opposition to said first deposition distribution of said first spacer insulating layer as a function of
8 said location of said split gate flash memory cell on said substrate.

1 7. The method as recited in Claim 6 wherein said composite spacer forms a composite
2 floating gate spacer proximate a floating gate of said split gate flash memory cell.

1 8. The method as recited in Claim 6 wherein said first spacer insulating layer forms a
2 thicker composition proximate a center of said substrate and a thinner composition toward an
3 edge of said substrate and said second spacer insulating layer forms a thinner composition
4 proximate said center of said substrate and a thicker composition toward said edge of said
5 substrate.

1 9. The method as recited in Claim 6 wherein said split gate flash memory cell is located
2 proximate a center of said substrate, said first spacer insulating layer having a thicker
3 composition and said second spacer insulating layer having a thinner composition.

1 10. The method as recited in Claim 6 wherein said first spacer insulating layer is formed by a
2 low pressure tetraethyl orthosilicate layer and said second spacer insulating layer is formed by a
3 plasma enhanced tetraethyl orthosilicate layer.

1 11. A split gate flash memory cell, comprising:

2 a substrate;

3 a substrate insulating layer overlying said substrate;

4 a floating gate overlying said substrate insulating layer;

5 a floating gate insulating layer overlying said floating gate; and

6 a composite floating gate spacer, including:

7 a first spacer insulating layer overlying said floating gate insulating layer and

8 having a first deposition distribution that varies as a function of a location of said split gate flash

9 memory cell on said substrate, and

10 a second spacer insulating layer overlying said first spacer insulating layer and

11 having a second deposition distribution that varies in substantial opposition to said first

12 deposition distribution of said first spacer insulating layer as a function of said location of said

13 split gate flash memory cell on said substrate.

1 12. The split gate flash memory cell as recited in Claim 11, further comprising:

2 a coupling spacer that extends between said floating gate and said substrate insulating

3 layer adjacent a source of said split gate flash memory cell; and

4 a composite contact spacer overlying said coupling spacer.

1 13. The split gate flash memory cell as recited in Claim 12, further comprising:

2 a common source line located adjacent said composite floating gate spacer and composite

3 contact spacer and overlying said source;

4 a tunneling insulating layer located adjacent said composite floating gate spacer on an

5 opposing side from said common source line;

6 a control gate located adjacent said tunneling insulating layer; and

7 a drain about said control gate and recessed into said substrate.

1 14. The split gate flash memory cell as recited in Claim 11 wherein said first spacer
2 insulating layer forms a thicker composition proximate a center of said substrate and a thinner
3 composition toward an edge of said substrate and said second spacer insulating layer forms a
4 thinner composition proximate said center of said substrate and a thicker composition toward
5 said edge of said substrate.

1 15. The split gate flash memory cell as recited in Claim 11 wherein said first spacer
2 insulating layer is formed by a low pressure tetraethyl orthosilicate layer and said second spacer
3 insulating layer is formed by a plasma enhanced tetraethyl orthosilicate layer.

1 16. A method of forming a split gate flash memory cell, comprising:
2 providing a substrate;
3 forming a substrate insulating layer over said substrate;
4 forming a floating gate over said substrate insulating layer;
5 forming a floating gate insulating layer over said floating gate; and
6 forming a composite floating gate spacer, including:
7 depositing a first spacer insulating layer over said floating gate insulating layer,
8 said first spacer insulating layer having a first deposition distribution that varies as a function of
9 a location of said split gate flash memory cell on said substrate, and
10 depositing a second spacer insulating layer over said first spacer insulating layer,
11 said second spacer insulating layer having a second deposition distribution that varies in
12 substantial opposition to said first deposition distribution of said first spacer insulating layer as a
13 function of said location of said split gate flash memory cell on said substrate.

1 17. The method as recited in Claim 16, further comprising:
2 forming a coupling spacer between said floating gate and a source of said split gate flash
3 memory cell; and
4 forming a composite contact spacer over said coupling spacer.

1 18. The method as recited in Claim 17, further comprising:
2 forming a common source line adjacent said composite floating gate spacer and
3 composite contact spacer and overlying said source;
4 forming a tunneling insulating layer adjacent said composite floating gate spacer on an
5 opposing side from said common source line;

6 forming a control gate adjacent said tunneling insulating layer; and
7 forming a drain about said control gate and recessed into said substrate.

1 19. The method as recited in Claim 16 wherein said first spacer insulating layer forms a
2 thicker composition proximate a center of said substrate and a thinner composition toward an
3 edge of said substrate and said second spacer insulating layer forms a thinner composition
4 proximate said center of said substrate and a thicker composition toward said edge of said
5 substrate.

1 20. The method as recited in Claim 16 wherein said first spacer insulating layer is formed by
2 a low pressure tetraethyl orthosilicate layer and said second spacer insulating layer is formed by
3 a plasma enhanced tetraethyl orthosilicate layer.

1 21. A composite spacer for use with a split gate flash memory cell on a substrate, comprising:
2 a first spacer insulating layer having a substantially uniform deposition distribution
3 across a surface thereof; and
4 a second spacer insulating layer overlying said first spacer insulating layer and having a
5 varying deposition distribution across a surface thereof, said second spacer insulating layer
6 having a thinner composition in selected regions of said split gate flash memory cell.

1 22. The composite spacer as recited in Claim 21 wherein said composite spacer forms a
2 composite contact spacer proximate a composite floating gate spacer of said split gate flash
3 memory cell.

1 23. The composite spacer as recited in Claim 21 wherein said selected region is a narrow
2 region between composite floating gate spacers of said split gate flash memory cell, said second
3 spacer insulating layer having a thinner composition therebetween.

1 24. The composite spacer as recited in Claim 21 wherein said first spacer insulating layer is a
2 hot temperature oxide layer.

1 25. The composite spacer as recited in Claim 21 wherein said second spacer insulating layer
2 is a resist protect oxide layer.

1 26. A method of forming a composite spacer for use with a split gate flash memory cell on a
2 substrate, comprising:

3 providing a first spacer insulating layer having a substantially uniform deposition
4 distribution across a surface thereof; and

5 depositing a second spacer insulating layer over said first spacer insulating layer, said
6 second spacer insulating layer having a varying deposition distribution across a surface thereof,
7 said second spacer insulating layer having a thinner composition in selected regions of said split
8 gate flash memory cell.

1 27. The method as recited in Claim 26 wherein said composite spacer forms a composite
2 contact spacer proximate a composite floating gate spacer of said split gate flash memory cell.

1 28. The method as recited in Claim 26 wherein said selected region is a narrow region
2 between composite floating gate spacers of said split gate flash memory cell, said second spacer
3 insulating layer having a thinner composition therebetween.

1 29. The method as recited in Claim 26 wherein said first spacer insulating layer is formed by
2 a hot temperature oxide layer.

1 30. The method as recited in Claim 26 wherein said second spacer insulating layer is formed
2 by a resist protect oxide layer.

1 31. A split gate flash memory cell, comprising:
2 a substrate;
3 a substrate insulating layer overlying said substrate;
4 a floating gate overlying said substrate insulating layer;
5 a floating gate insulating layer overlying said floating gate; and
6 a composite contact spacer located proximate said floating gate, including:
7 a first spacer insulating layer having a substantially uniform deposition
8 distribution across a surface thereof, and
9 a second spacer insulating layer overlying said first spacer insulating layer and
10 having a varying deposition distribution across a surface thereof, said second spacer insulating
11 layer having a thinner composition in selected regions of said split gate flash memory cell.

1 32. The split gate flash memory cell as recited in Claim 31, further comprising:
2 a coupling spacer that extends between said floating gate and said substrate insulating
3 layer adjacent a source of said split gate flash memory cell and underlying said composite
4 contact spacer; and
5 a composite floating gate spacer overlying said floating gate insulating layer.

1 33. The split gate flash memory cell as recited in Claim 32, further comprising:
2 a common source line located adjacent said composite floating gate spacer and composite
3 contact spacer and overlying said source;
4 a tunneling insulating layer located adjacent said composite floating gate spacer on an
5 opposing side from said common source line;
6 a control gate located adjacent said tunneling insulating layer; and
7 a drain about said control gate and recessed into said substrate.

1 34. The split gate flash memory cell as recited in Claim 31 wherein said selected region is a
2 narrow region adjacent a composite floating gate spacer of said split gate flash memory cell, said
3 second spacer insulating layer having a thinner composition therebetween.

1 35. The split gate flash memory cell as recited in Claim 31 wherein said first spacer
2 insulating layer is a hot temperature oxide layer and said second spacer insulating layer is a resist
3 protect oxide layer.

1 36. A method of forming a split gate flash memory cell, comprising:
2 providing a substrate;
3 forming a substrate insulating layer over said substrate;
4 forming a floating gate over said substrate insulating layer;
5 forming a floating gate insulating layer over said floating gate; and
6 forming a composite contact spacer proximate said floating gate, including:
7 providing a first spacer insulating layer having a substantially uniform deposition
8 distribution across a surface thereof, and
9 depositing a second spacer insulating layer over said first spacer insulating layer,
10 said second spacer insulating layer having a varying deposition distribution across a surface
11 thereof, said second spacer insulating layer having a thinner composition in selected regions of
12 said split gate flash memory cell.

1 37. The method as recited in Claim 36, further comprising:
2 forming a coupling spacer between said floating gate and a source of said split gate flash
3 memory cell and underlying said composite contact spacer; and
4 forming a composite floating gate spacer over said floating gate insulating layer.

1 38. The method as recited in Claim 37, further comprising:
2 forming a common source line adjacent said composite floating gate spacer and
3 composite contact spacer and overlying said source;
4 forming a tunneling insulating layer adjacent said composite floating gate spacer on an
5 opposing side from said common source line;
6 forming a control gate adjacent said tunneling insulating layer; and
7 forming a drain about said control gate and recessed into said substrate.

1 39. The method as recited in Claim 36 wherein said selected region is a narrow region
2 adjacent a composite floating gate spacer of said split gate flash memory cell, said second spacer
3 insulating layer having a thinner composition therebetween.

1 40. The method as recited in Claim 36 wherein said first spacer insulating layer is formed by
2 a hot temperature oxide layer and said second spacer insulating layer is formed by a resist protect
3 oxide layer.

1 41. A coupling spacer for use with a split gate flash memory cell on a substrate having a
2 substrate insulating layer thereon comprising a conductive layer that extends between a floating
3 gate and said substrate insulating layer adjacent a source recessed into said substrate of said split
4 gate flash memory cell.

1 42. The coupling spacer as recited in Claim 41 wherein said conductive layer is doped
2 polycrystalline silicon.

1 43. The coupling spacer as recited in Claim 42 wherein said doped polycrystalline silicon has
2 a thickness of about 200 angstroms.

1 44. The coupling spacer as recited in Claim 41 wherein said coupling spacer is located
2 proximate a composite floating gate spacer of said split gate flash memory cell.

1 45. The coupling spacer as recited in Claim 41 wherein said coupling spacer underlies a
2 composite contact spacer of said split gate flash memory cell.

1 46. A method of forming a coupling spacer for use with a split gate flash memory cell on a
2 substrate having a substrate insulating layer thereon comprising forming a conductive layer that
3 extends between a floating gate and said substrate insulating layer adjacent a source recessed into
4 said substrate of said split gate flash memory cell.

1 47. The method as recited in Claim 46 wherein said conductive layer is doped polycrystalline
2 silicon.

1 48. The method as recited in Claim 47 wherein said doped polycrystalline silicon has a
2 thickness of about 200 angstroms.

1 49. The method as recited in Claim 46 wherein said coupling spacer is located proximate a
2 composite floating gate spacer of said split gate flash memory cell.

1 50. The method as recited in Claim 46 wherein said coupling spacer underlies a composite
2 contact spacer of said split gate flash memory cell.

1 51. A split gate flash memory cell, comprising:
2 a substrate;
3 a source recessed into said substrate;
4 a substrate insulating layer overlying said substrate;
5 a floating gate overlying said substrate insulating layer;
6 a floating gate insulating layer overlying said floating gate; and
7 a coupling spacer including a conductive layer that extends between said floating gate
8 and said substrate insulating layer adjacent said source.

1 52. The split gate flash memory cell as recited in Claim 51, further comprising:
2 a composite floating gate spacer overlying said floating gate insulating layer; and
3 a composite contact spacer located proximate said composite floating gate spacer.

1 53. The split gate flash memory cell as recited in Claim 52, further comprising:
2 a common source line located adjacent said composite floating gate spacer and composite
3 contact spacer and overlying said source;
4 a tunneling insulating layer located adjacent said composite floating gate spacer on an
5 opposing side from said common source line;
6 a control gate located adjacent said tunneling insulating layer; and
7 a drain about said control gate and recessed into said substrate.

1 54. The split gate flash memory cell as recited in Claim 51 wherein said conductive layer is
2 doped polycrystalline silicon having a thickness of about 200 angstroms.

1 55. The split gate flash memory cell as recited in Claim 51 wherein said coupling spacer
2 underlies a composite contact spacer of said split gate flash memory cell.

1 56. A method of forming a split gate flash memory cell, comprising:
2 providing a substrate;
3 forming a source recessed into said substrate;
4 forming a substrate insulating layer over said substrate;
5 forming a floating gate over said substrate insulating layer;
6 forming a floating gate insulating layer over said floating gate; and
7 forming a coupling spacer including a conductive layer that extends between said floating
8 gate and said substrate insulating layer adjacent said source.

1 57. The method as recited in Claim 56, further comprising:
2 forming a composite floating gate spacer over said floating gate insulating layer; and
3 forming a composite contact spacer proximate said composite floating gate spacer.

1 58. The method as recited in Claim 57, further comprising:
2 forming a common source line adjacent said composite floating gate spacer and
3 composite contact spacer and overlying said source;
4 forming a tunneling insulating layer adjacent said composite floating gate spacer on an
5 opposing side from said common source line;
6 forming a control gate adjacent said tunneling insulating layer; and
7 forming a drain about said control gate and recessed into said substrate.

1 59. The method as recited in Claim 56 wherein said conductive layer is doped polycrystalline
2 silicon having a thickness of about 200 angstroms.

1 60. The method as recited in Claim 56 wherein said coupling spacer underlies a composite
2 contact spacer of said split gate flash memory cell.